UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,282	03/30/2004	Yasutaka Nakashiba	8008-1052	2273

466 7590 08/13/2009

YOUNG & THOMPSON
209 Madison Street
Suite 500
ALEXANDRIA, VA 22314

EXAMINER	
JACKSON JR, JEROME	
ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
08/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,282	NAKASHIBA, YASUTAKA	
	Examiner	Art Unit	
	Jerome Jackson Jr.	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 23-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo in view of O and further in view of APA, of record.

The previous rejection still applies. The new claims are not patentable because the prior art has recognized:

1. Varactors are made from CMOS structures and use the smallest gate oxide thickness (O);

2. Integrated circuitry with low power and high power MOSFETs are designed with gate oxides of different thicknesses (Kudo and O);

3. Wiring NMOS transistors for varactor operation is well known (O and APA);

4. Applicant's claimed structure would not distinguish over the obvious structure suggested by the applied art where varactors are integrated with MOSFETs, and where the varactor oxide thickness is thinner than I/O MOSFET oxide thickness. See column 10 of O below:

Varactors are used for tuning filters and implementing low phase noise voltage controlled oscillators (VCO). A varactor is a semiconductor device (often a FET) in which the capacitance is sensitive to the applied voltage. A varactor can be formed by positioning an NMOS transistor in an n-well [C.-M. Hung, I-C. Wu, Y.-C. Ho, and K. K. O, "High Q Capacitors (>150 @900 MHz) Implemented in a CMOS Process for Wireless Applications," ISEE Transaction on MTT, vol. 46, no. 5, pp 505--511, May, 1998.]. This arrangement creates a short between the source, well and drain.

At 24 GHz, the varactor Q is expected to be about 30, which will limit the performance of filters and the VCO. When the frequency is increased beyond 24 GHz, the situation will become worse.

CMOS varactors are generally formed using design rules applicable for logic devices, as opposed to design rules for input/output (I/O) devices. Logic devices are generally significantly smaller than I/O devices, and use a thinner gate oxide.

To improve the Q of varactors, the invention provides several design approaches including patterning high voltage transistor structures with a lower capacitance/area using the finer line patterning available for low voltage (e.g. 100 nm) gate length transistors typically used for logic devices.

The Q of a varactor is proportional to 1/CRω, where ω is the angular frequency. In a conventional CMOS process, the gate oxide is relatively thick for I/O devices and thin for logic devices. The maximum Q of the varactor formed from an NMOS device in an N-well is limited by n-well resistance and capacitance of the smallest varactor that can be defined in a given process technology. This is limited by the minimum dimensions allowed in a given technology. Larger varactors can be constructed by putting this smallest varactors in parallel while maintaining the maximum Q. Both capacitance and resistance should be as low as possible to achieve high Q. Thus, the invention uses the thicker gate oxide ordinarily used for I/O devices, with a short channel length. Short length provides low resistance, while thick gate oxide lowers capacitance. Operating frequency of varactors can be from hundreds of MHz to 100 GHz and higher.

Above, O discloses varactors are formed from logic NMOS structures and are smaller than I/O MOSFETs, and particularly use smaller gate oxide thicknesses. Accordingly, there is nothing novel having varactors with the smallest oxide thickness integrated with other integrated MOS transistors (I/O) having thicker oxide. Claim 36 is obvious structure.

Applicant's arguments filed 5/4/09 have been fully considered but they are not persuasive. Applicant's first argument is the art as a whole does not teach, suggest nor disclose a varactor oxide thinner than MOSFET oxide devices integrated with it.

In rebuttal, as stated above, varactors typically have the thinnest oxide and are designed from the thinnest MOSFET structures. Therefore the varactors have thinner oxides than thicker oxide I/O MOSFETs integrated with the varactors. Kudo also discloses I/O (higher threshold) transistors comprising a second and third gate oxide both with thicker oxides than the thinnest logic (lower threshold) FETs. Accordingly, the prior art teaches or suggests a prima facie obvious structure wherein varactor oxide thickness is thinner than at least I/O (higher threshold) transistors comprising at least two additional type MOSFET transistors both with thicker oxides than the varactor device. This structure alone makes claims 23 and 36 prima facie obvious structures. Notwithstanding there may be additional "logic" transistors on the integrated chip with oxides as thin as the varactors, the fact there are additional transistors with thicker oxides than the varactor device, the claims are not patentable.

Applicant's stumbling block appears to be the definition of "MOS transistors" in the claims relative to "MOS type varactor element". Applicant argues "all of the MOS transistors" must be greater than the varactor element. First, "all" is relative here and it is not in the claims. Secondly, "all" could be defined as all of the I/O (higher threshold) transistors of the prior art. The claims do not distinguish over the applied art.

Applicant argues the "MOS transistor" does not have the varactor structure. This argument is unconvincing as the prior art well recognizes varactors are formed from MOS transistor structures. See O and APA. Applicant was not the first to form a varactor from a MOSFET or wire a MOSFET to function as a varactor.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson Jr. whose telephone number is 571-272-1730. The examiner can normally be reached on M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815